REMARKS/ARGUMENTS

Claims 1-20 and 25 are pending. Claims 1, 7, 13, and 19 have been amended. Claims 21-24 have been canceled. Support for the amended claims is found in the specification. No new matter has been added.

Claims 1-20 and 25 are rejected under 35 U.S.C. § 102(e) as being anticipated by Novak (6,295,586). The applicants respectfully request reconsideration and allowance of the claims.

Claim Rejections - 35 U.S.C. § 102(e)

The claims are allowable because each and every element is not shown or suggested by the prior art. For example, claim 1 recites, "an arbiter simultaneously coupled to each of the plurality of memory transactions and configured to generate a plurality of bank readiness signals."

As described in the specification, the "present invention relates generally to interconnection architecture, and particularly to interconnecting multiple processors with multiple shared memories." (Specification at page 1, lines 2-3). In one embodiment, a queue includes a plurality of request stations 112A through 112N, each request station storing a memory transaction destined for one of a plurality of memory banks. As illustrated in figure 2, the arbiter is simultaneously coupled to each of the plurality of memory transactions and generates bank readiness signals BNKRDYA through BNKRDYM. The arbiter selects one of the memory transactions from the queue based on the readiness of the memory banks to accept a memory transaction. (Specification at page 4, lines 19-30 and Figure 2). Because the arbiter is simultaneously coupled to each of the plurality of memory transactions, the selection of a memory transaction is not limited the memory transaction stored in the final request station, for example, request station 112N in figure 2. (See Specification at page 11, lines 13-25 and figure 7).

In contrast, Novak appears to discuss several queues (AQ, PQ, and RWQ) that are independently connected to the multiplexer SPM 370. (Novak at col. 8, line 66 to col. 9, line 5 and figure 2). As illustrated in figure 2 of Novak, only the bottom entry of each queue is connected to the multiplexer SPM. Taking the RWQ as an example, only the bottom entry of the

RWQ is connected to the SPM. Thus, only a subset of the queue entries (the bottom entries) are simultaneously coupled to the SPM.

Therefore, in contrast with the present invention, Novak fails to teach or suggest "an arbiter simultaneously coupled to each of the plurality of memory transactions and configured to generate a plurality of bank readiness signals," as recited by claim 1. For at least these reasons, claim 1 is in a condition for allowance.

Claims 2-6

Claims 2-6, which depend from claim 1, are in a condition for allowance, for at least the reasons discussed in relation to claim 1, as well as for the additional limitations they recite.

Claim 7

Claims 7 recites "generating a plurality of bank readiness signals by monitoring the addresses of the plurality of memory transactions gated across the memory bus at a location along the memory bus." As illustrated in figure 2 of the specification, in one embodiment, the state machine 204 "monitors the addresses of the memory transactions that are gated to memory 104" over memory bus 106 at a location along the memory bus. (Specification at page 5, lines 14-15).

Novak, on the other hand, discusses a memory controller in which "[e]ach of the operation queues 340, 350, 360 are operation requesters." The operation queues "assert a signal to the SPM" that "tells the SPM 370 that there is an operation ready to be sent." (Novak at col. 11, lines 11-15, emphasis added). Thus, Novak appears to disclose a memory controller with operation queues AQ, PQ and RWQ operative to generate ready signals. However, as illustrated in figure 2 of Novak, these operation queues do not monitor the addresses of memory transactions gated across the memory bus at a location along the memory bus. On the contrary, the operation queues are located upstream of the SPM and are not operable to monitor the addresses of memory transactions at a location along the memory bus. Because at least these claim elements are not taught or suggested by the prior art, claim 7 is in a condition for allowance.

Claims 8-12

Claims 8-12, which depend from claim 7, are in a condition for allowance, for at least the reasons discussed in relation to claim 7, as well as for the additional limitations they recite.

Claim 13

Claim 13 recites "means for generating a plurality of bank readiness signals based upon a content of the memory bus using an arbiter simultaneously coupled to each of the plurality of memory transactions, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction." As discussed in relation to claim 1, Novak fails to teach or suggest at least these claim limitations. For at least these reasons, claim 13 is in a condition for allowance.

Claims 14-18 and 20

Claims 14-18 and 20, which depend from claim 13, are in a condition for allowance, for at least the reasons discussed in relation to claim 13, as well as for the additional limitations they recite.

Claim 19

Claim 19 recites a "computer program product," "the product comprising instructions operable to cause a programmable processor to:" "generate a plurality of bank readiness signals based upon a content of the memory bus by monitoring the addresses of the plurality of memory transactions gated across the memory bus at a location along the memory bus." As discussed in relation to claim 7, Novak fails to teach or suggest at least these claim limitations. For at least these reasons, claim 19 is in a condition for allowance.

Claim 25

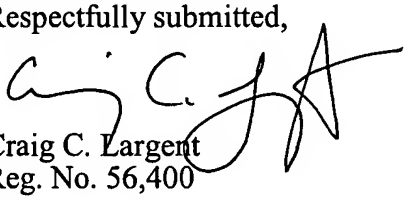
Claim 25, which depends from claim 19, is in a condition for allowance, for at least the reasons discussed in relation to claim 19, as well as for the additional limitations it recites.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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